REMARKS

This is in response to the Office Action of 04 October 2004. Claims 1-20 are pending in the application, and Claims 1-20 have been rejected.

By this Response and Amendment, the Specification is amended, Claims 4-11, and 14-20 are amended, and arguments traversing various rejections are presented.

No new matter has been added.

In view of the amendments above and remarks below, Applicants respectfully request reconsideration and further examination.

About The Invention

The present invention relates generally to methods and apparatus for generating random numbers. More particularly, the present invention relates to modifying the frequency of at least one frequency generator circuit which feeds into a logic network that computes parity for a first predetermined number of clock cycles, and further relates to collecting the output of the logic network after the first predetermined number of clock cycles, until a second predetermined number of bits have been collected.

Specification

The specification has been amended such that the first paragraph thereof does not refer to specific Claims.

Priority

The Examiner states that Applicants have not filed a certified copy of the 10000502.0 application as required by 35 USC §119(b). Additionally, the Examiner has requested an English translation of the German document.

Applicants' file records indicate that the priority document was filed with the initial application papers. Further, the Office Action Summary sheet indicates that some certified copies of the priority documents have been received. Applicants respectfully request that the requirement to re-file priority documents be withdrawn.

With respect to providing an English translation for the German document, Applicants respectfully note that there is no need to rely upon the priority document to overcome the references presently cited against the Claims. In view thereof Applicants' respectfully request the Examiner to reconsider and withdraw the request for a translation at this time.

Claim Objections

Claims 5-20 have been objected to as being of improper dependent form.

By this Response, Claims 5-10 have been amended to depend from Claim 2; Claim 11 has been amended to be in independent form; and Claims 14-20 have been amended to depend from independent Claim 11. Applicants respectfully submit that these amendments overcome the objection to Claims 5-20.

Rejections under 35 USC §112, second paragraph

Claims 5-20 have been rejected under 35 USC §112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

By this Response, Claims 5-10 have been amended to depend from Claim 2; Claim 11 has been amended to be in independent form; and Claims 14-20 have been amended to depend from independent Claim 11. Applicants respectfully submit that by removing the improper multiple dependencies noted

by the Examiner, the rejections under 35 USC §112, second paragraph have been overcome.

Rejections under 35 USC §102(e)

Claims 1-20 have been rejected under 35 USC §102(e) as being anticipated by Ogrodski (US Patent 4,799,259).

Claims 1-4, 7-8, 11-14, and 17-18 have been rejected under 35 USC §102(e) as being anticipated by Le Quere (US Patent 6,714,955).

As set forth more fully below, Applicants respectfully traverse the rejection of Claims 1-20 as being anticipated by Ogrodski under 35 USC §102(e), and request that these rejections be withdrawn.

Independent Claims 1 and 11 both recite limitations regarding the parity circuit (20) generating or determining the parity for a predetermined number (Nlog) of clocks. It is this parity value, i.e., the parity after Nlog clocks, that forms a single bit of data for the random number register. Applicants' claimed parity circuit (20) is clearly different from that disclosed by Ogrodski. All the parity circuits shown by Ogrodski consist of combinatorial logic, and are not clocked as is the parity circuit (20) of Applicants' invention. It is clear that a clock input is used by Applicants' claimed parity circuit (20) because this circuit must determine when Nlog clocks' worth of parity computation has been completed. The parity bit resulting after Nlog clocks of parity generation is stored in the claimed random number register (22) which is capable of storing Nz bits of output from parity circuit (20). Ogrodski's combinatorial parity network changes its result on every clock, which is unlike Applicants' claimed Nlog clocks.

For at least the foregoing reasons, Applicants respectfully submit that the rejection based on Ogrodski under 35 USC §102(e), of independent Claims 1 and 11, along with the Claims that respectively depend therefrom, has been overcome.

Further, Applicants submit that Ogrodski does not suggest or provide motivation for Applicants' claimed invention.

As set forth more fully below, Applicants respectfully traverse the rejection of Claims 1-4, 7-8, 11-14, and 17-18 as being anticipated by Le Quere under 35 USC §102(e), and request that these rejections be withdrawn.

Applicants respectfully submit that Le Quere is an improper reference under 35 USC §102(e) because the International Application (WO01/46797) was not published in the English language as required by the statute, but rather was published in the French language. MPEP §706.02(f)(1)(III) further illustrates that the Le Quere reference is improper under 35 USC §102(e) because of publication in French rather than English.

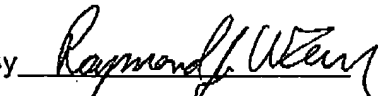
For at least the foregoing reasons, Applicants respectfully request that the rejections based on Le Quere be withdrawn.

Conclusion

All of the objections and rejections in the outstanding Office Action of 08 October 2004 have been responded to, and Applicants respectfully submit that the pending Claims 1-20 are now in condition for allowance.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

By 

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Hillsboro, Oregon

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